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Developments of Novel Vertically Integrated Pixel Sensors in the High Energy Physics Community

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***Abstract*–High energy physics experiments at future particle accelerators set very demanding requirements on the performance of sensors and readout electronics. In these applications, silicon pixel detectors have to integrate advanced functionalities in the pixel cell itself, such as amplification, filtering, discrimination, time stamping, zero suppression and analog-to-digital conversion. This paper discusses how 3D vertical integration has the potential of providing a performance breakthrough in particle detection systems, and how the high energy physics community is organizing itself to meet the challenges of designing and fabricating vertically integrated devices.**

I. Introduction

VERTICAL integration technology is going to play an important role in the design of advanced silicon pixel sensors in future high energy physics experiments at particle accelerators. In these applications, a fundamental problem will be the reconstruction of charged particle tracks with high resolution sensors. These sensors, along with the readout electronics, will be required to have a small pixel pitch (≤ 20 μm in some applications), a high degree of radiation tolerance, a large signal-to-noise ratio, a low mass to minimize particle scattering, a low power dissipation and the capability of handling very high data rates. This paper presents the novel design solutions that are being pursued by the high energy physics scientific community in the framework of international collaborations with the goal of advancing the state of the art of pixel sensors and meeting these demanding specifications.

Three main research lines are being followed to exploit vertical integration. The first one can be seen as a development of the classical MAPS (Monolithic Active Pixel Sensors) concept of signal charge generation and collection by diffusion in an undepleted silicon region. In this case vertical integration of two (or more) CMOS layers makes it possible to separate the analog front-end electronics from the digital readout sections, with great advantages in terms of pixel size, functionalities and performance. Complex functions are integrated in the pixel cell itself, such as low-noise amplification, sparsified readout (zero suppression) and time stamping. Different readout architectures have been designed to handle a large data flow without the constraints that may arise when digital electronics is implemented on the same substrate as the sensor (as in standard MAPS).

The second research line is based on SOI (Silicon-On-Insulator) technology, where the handle wafer forms the radiation sensor and the readout electronics is implemented in the top wafer. The SOI technology is well suited to vertical integration, so several SOI wafers can be stacked without major problems.

The third R&D line explores the possibility of using vertical integration to interconnect layers fabricated in different technologies, i.e. to connect a sensor built in a fully-depleted high resistivity silicon substrate to readout electronics fabricated in an ultra deep submicron (130 nm or below) CMOS process. This can provide a large benefit in terms of radiation hardness and signal-to-noise ratio.

Vertically integrated pixel sensors may cover a broad range of applications besides particle tracking in high energy physics experiments. Imagers for advanced X-ray sources may strongly benefit from the improved functionalities and performance that come with vertical integration and allow for small pitch pixels capable of handling high data rates. To meet the challenges associated with design, fabrication and testing of 3D vertically integrated pixel sensors, the particle detector community has organized itself in various consortia, with the goal of tackling different technologies and design solutions. As discussed in this paper, the community has also set up a mechanism to facilitate collaboration in the area of vertically integrated system designs and to expedite enabling this technology for future high-energy physics experiments and projects in associated fields.

II. Vertically Integrated MAPS in Bulk CMOS

In presently operating high energy physics facilities such as the Large Hadron Collider (LHC), the sensor layers located closest to the particle interaction point are based on the "hybrid pixel" concept [1]. Here the detector is built in a high resistivity silicon wafer, and is driven into full depletion by applying an electric field between pixelated sensing electrodes and a back contact. Detectors are connected to readout integrated circuits (fabricated in commercial CMOS technologies) by bump bonding techniques, according to the concept shown in Fig. 1. In the electronics elementary cell (same size as the pixel electrodes), advanced functions are performed to cope with signal-to-noise ratio and high data rate requirements. These functions include amplification, filtering, calibration, threshold adjustment, analog-to-digital conversion, zero suppression (also called data sparsification) and time stamping, all carried out inside a single pixel cell. Since most of the present readout chips are built in 250 nm CMOS technologies, this architecture sets a lower limit on the pixel cell size, which, together with bump bonding constraints, prevents a reduction of the pixel pitch below 50 μm and a pixel area below 15,000 μm^2.

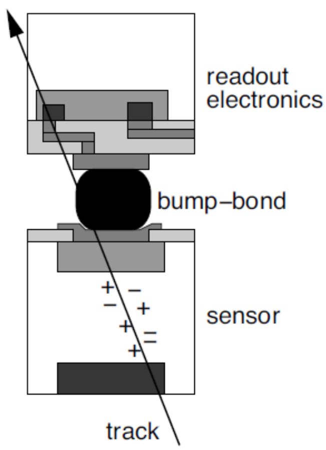

Fig. 1. Hybrid pixel structure [1], with CMOS readout chip and high-resistivity silicon sensor connected by a conductive bump.

To improve resolution, the next generation of high energy physics experiments demands a shrinking of the pixel size, without giving up electronic functionalities or even increasing them. A decrease of the amount of material in the system is also necessary to reduce errors in track reconstruction due to multiple scatterings of particles in the detectors. Future pixel systems will be required to detect smaller signals with respect to existing devices, because the active sensing layer will be thinned for material reduction or, in thick sensors, very high radiation levels will degrade charge collection properties.

MAPS provide an interesting solution to the problem of material reduction, because the monolithic integration of sensors and electronics removes the material associated with the bump bonding. Moreover, the sensors themselves can be thinned to a few tens of μm, since in standard MAPS signal charge is collected by diffusion to an N-type electrode from an epitaxial layer with a maximum thickness of 15-20 μm. Actually, since several years, MAPS have demonstrated their capability to perform charged particle tracking [2]. The MIMOSA chips series is an excellent example of a successful R&D program with the aim of extending MAPS applications to particle detection [3]. Such successful results opened up the possibility of using these devices in high energy physics applications. However, the standard MAPS architecture has several limitations. First of all, it is difficult to integrate advanced functionalities in the pixel cell, since PMOSFETs are avoided; they are located inside N-type wells which compete for charge collection with the signal electrode, and degrade the fill factor. Moreover, a charge collection mechanism relying on diffusion only has several drawbacks in terms of device speed, radiation hardness and signal-to-noise ratio. Nevertheless, clever solutions were found to implement amplification, filtering based upon correlated double sampling, and discrimination inside the pixel cells [3].

The high energy physics community is pursuing innovative solutions in monolithic pixel design to overcome the intrinsic limitations of MAPS, with the goal of improving the quality of the sensor substrate, the charge collecting properties of sensing electrodes and the performance of the readout electronics. As for the substrate, the ultimate goal is to use high-resistivity, fully-depleted silicon. In this respect, the most mature solution is presently the DEPFET [4], where electrons generated in a fully-depleted bulk steer the current in an amplifying transistor integrated in the pixel cell. Other solutions are driven by the implementation of advanced electronic functions (such as in hybrid pixels) inside the MAPS cell, which requires full CMOS circuits. To this purpose and to avoid an excessive degradation of charge collection, different ideas are being developed, such as using deep P-wells to shield the N-type wells which contain PMOSFETs [5]. In another approach, deep N-wells act as sensing electrodes extending over a large portion of the pixel, so that their area is much larger than the area taken by the PMOS N-wells [6]. The first front-end electronics stage is a charge-sensitive preamplifier, whose gain is set by its feedback capacitance and is decoupled from the value of the sensor capacitance, which is considerably higher than in standard MAPS with small charge collecting electrodes.

Although these developments have already achieved excellent results or are very promising, 3D vertical integration technologies appear to be extremely attractive for the development of monolithic pixel devices. A multilayer sensor structure (with thin layers interconnected by vertical vias) promises to overcome typical limitations of MAPS. In a 3D MAPS device, for example, a layer may host sensing electrodes and analog circuits, whereas digital electronics may be located in upper layers. In this way, most (if not all) the PMOSFETs and their competitive N-wells may be removed from the sensor layer, in principle achieving a 100% fill factor. A multilayer structure allows also for a smaller pixel pitch and a smaller sensor capacitance, leading to a better trade-off between noise and power dissipation. The removal of layout constraints related to efficiency problems may also have a beneficial impact on the digital readout architecture, adding more complex functionalities and increasing flexibility. As it will be discussed in more detail in Section IV, vertical integration also opens up the possibility of using different technologies for the sensor (high resistivity, detector-grade silicon) and for the readout electronics (deep submicron or even sub-100 nm CMOS) [7].

A 3D-IC Consortium [8] was promoted by Fermi National Accelerator Laboratory, to explore various issues associated to vertical integration. European and U.S. institutions are presently members of this Consortium, which, as a first step, is going to investigate 3D devices based on two layers ("tiers") of the 130 nm CMOS technology by Chartered Semiconductor, vertically integrated with the Tezzaron interconnection technology [9]. In the framework of this Consortium, it was possible to gather a pool of physicists and IC designers with the critical mass, competence and willingness to share knowledge that is necessary for such an ambitious enterprise. In the first Tezzaron/Chartered run organized by the Consortium, prototype devices will cover a broad range of architectures and applications. They include MAPS with digital readout separated from the sensor and the analog front-end, among which are more classical structures with small sensing diodes [10] and a rolling-shutter, parallel-column readout of the pixel matrix, as well as less standard devices with large deep N-well sensing electrodes connected to charge-sensitive preamplifiers [11] and a binary readout with pixel-level sparsification based on a token passing scheme. As an example, Fig. 2 shows how a deep N-well MAPS evolves from a standard two-dimensional CMOS implementation to a 3D vertically integrated two-tier device.

Two-tier readout electronic chips have also been designed, again according to different specifications and design solutions, with the general aim of implementing small readout pixel cells with advanced analog and digital signal processing features [12, 13]. Actually, the first 3D electronic chip (called VIP1) developed inside the high energy physics community was designed by Fermilab in the Fully-Depleted (FD) SOI 180 nm process by MIT Lincoln Laboratories [7]. It had three tiers of stacked electronics for the readout of 4096 pixels with a 20 μm pitch, including all the advanced analog and signal processing features that were previously discussed. A new version of this design was transferred to the Tezzaron/Chartered technology. The 3D chips fabricated in this first Tezzaron/Chartered run will be used for the readout of high-resistivity silicon sensors for high energy physics and X-ray imaging applications, as it will be thoroughly discussed in Section IV. The Consortium is actually interested in expanding its scope beyond particle tracking applications, considering that imagers for advanced X-ray sources may strongly benefit from vertical integration. One of the advantages which may extend to imaging is the possibility to build 4-side buttable devices, with I/O pads on the backside, connected by through-silicon vias. This, in principle, enables fabrication of pixel detectors with large area coverage without any dead space [14]. The two-tier devices of the first run organized by the 3D-IC Consortium will be built using a face-to-face bond of two wafers, as shown in Fig. 3. To reduce mask costs, a single set of masks will include both the top and bottom circuits. Fabrication starts in July '09: because of the wide range of devices that are going to be integrated, this run is expected to provide extensive information about vertically integrated pixelated devices and to be the basis for future developments in the community.

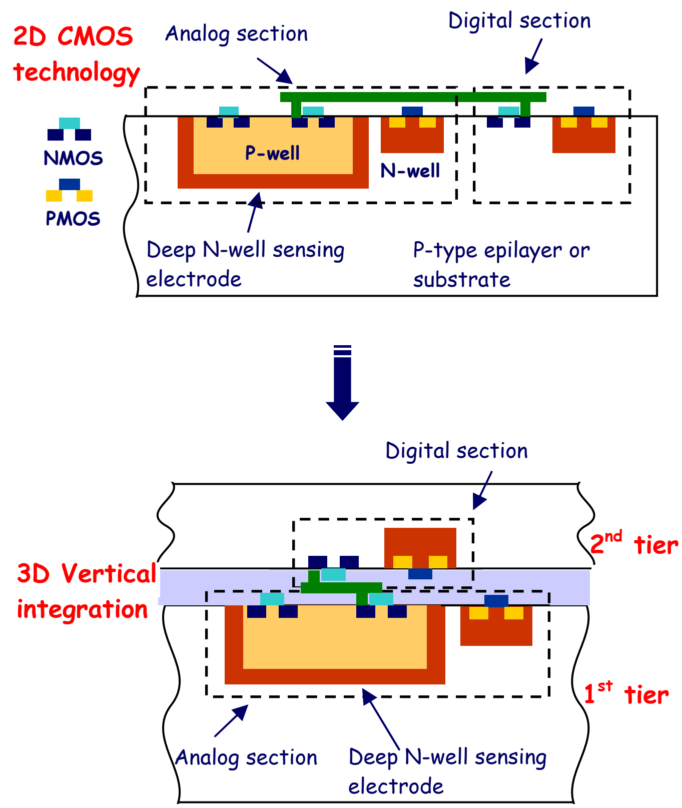

Fig. 2. Conceptual evolution of a MAPS device with deep N-Well sensing electrodes from a 2D standard CMOS technology to a 3D vertically integrated structure.

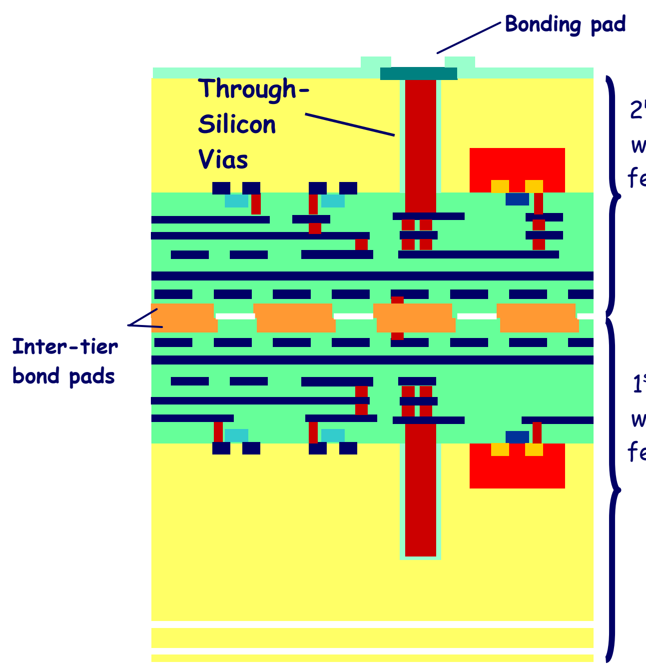

Fig. 3. 3D devices resulting from stacking and bonding two 130 nm CMOS wafers by Chartered using the vertical integration technology by Tezzaron.

III. SOI SENSORS AND VERTICAL INTEGRATION

Most of the recent SOI wafers are fabricated by bonding two different wafers [15]. Therefore it can be possible to fabricate a radiation sensor in the bottom (handle) wafer by using high-resistivity Si while implementing conventional CMOS circuits in the top (SOI) Si [16], as shown in Fig. 4. To fabricate P-N junctions in the handle wafer and connect the sensor signals to the readout circuits through the buried oxide (BOX) layer, a new SOI pixel process was developed based on the 0.2 μm FD SOI process of OKI Semiconductor Co. Ltd. [17, 18].

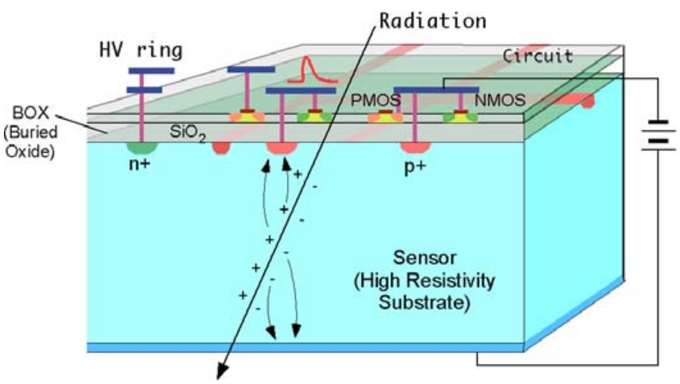

Fig. 4. Cross sectional view of a SOI pixel detector.

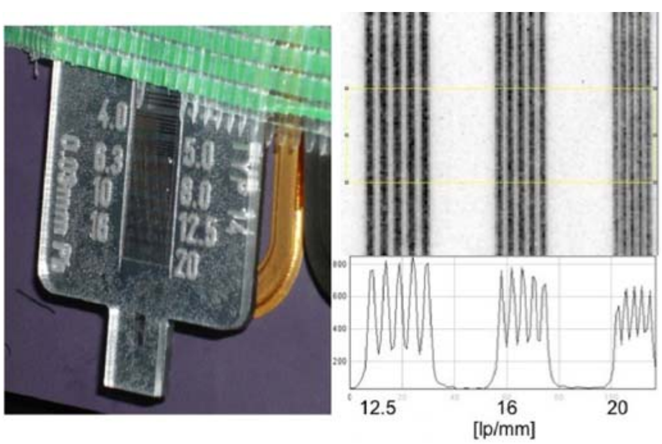

Fig. 5. An example of an X-ray test chart image taken with the SOI pixel chip. The pixel size is 20 μm by 20 μm, and there are 128 x 128 pixels in the chip. The energy of the X-ray is about 8 keV.

Figure 5 shows an example of an X-ray test chart image taken with the SOI pixel. To reduce the development cost of a design, MPW (Multi Project Wafer) runs are organized periodically within our community [19].

Advantages of the SOI pixel detector are the following:

- No mechanical bump bonding, so obstacles which will cause multiple scattering are minimized and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10 fF), so large conversion gain and low noise are possible.
- Full CMOS circuitry can be implemented in each pixel.
- The technology is based on industry standards, so further progress and lower cost is envisaged.

While the SOI structure is ideal for realizing the monolithic pixel detector, there are some issues relating to couplings between the sensor and the electronics due to their very close placement. To mitigate the coupling, two technologies are being developed. One is a P-type implantation without removing the top Si layer (Buried P-Well: BPW); the other is an additional vertical integration with a μ-bump technique.

The BPW region will help to reduce the so-called back gate effect and charge trapping in the BOX, will improve the break-down voltage and will provide sensor design flexibility. The doping level of the BPW is about 3 orders of magnitude lower than that of the P^+ sensor node and of the drain/source regions, and we confirmed that there is no visible change in the transistor characteristics.

To increase circuit density further, we are also pursuing bonding of two SOI wafers face-to-face by using the μ-bump technology of ZyCube Co. Ltd [20]. A cross sectional view of the bonded chip is shown in Fig. 6. Minimum pitch of the bump is 5 μm. This will enable higher circuit integration density and separate the sensitive circuit regions from the sensors. After bonding two SOI wafers, the upper handle wafer is removed and I/O pad are created. This structure is ideal for a back illumination detector having 100% effective area.

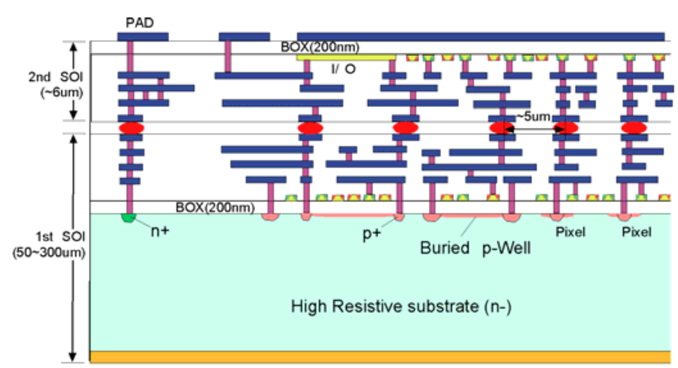

Fig. 6. SOI wafer cross section with buried P-well structures.

IV. VERTICAL INTEGRATION BETWEEN HIGH RESISTIVITY SILICON SENSORS AND CMOS READOUT ELECTRONICS

Sensors can be integrated in one tier of the 3D multilayer structure as demonstrated with the MAPS technology, described in Section II. The previous section illustrated the integration of a sensor and front-end electronics in single SOI technology. Vertical integration can also be used to interconnect layers fabricated in different technologies, e.g. to connect a sensor built in a fully-depleted high resistivity silicon substrate to readout electronics fabricated in a commercial ultra deep submicron process. Note that the readout electronics itself may already be produced in a 3D process. The challenge then is the formation of a strong, reliable, low-mass bond between the sensor and the readout electronics. To date, three 3D techniques have been explored for sensor and ROIC (ReadOut Integrated Circuit) integration to overcome the limitations of the current bump bond technology for hybrid pixels.

The first approach was a modification of the conventional bump bonding technology, carried out with RTI to demonstrate the feasibility of bonding at a pitch less than 20 μm [21]. Two processes were studied: small interconnect pillars of CuSn bonded to Cu and SnPb pillars bonded to Ni/Au. The bond yield of the CuSn bonding was in excess of 99.995% with bumps of about 10 μm in diameter, thus establishing the feasibility of CuSn bonding for fine pitch assembly of 3D circuits. A cross section of the RTI CuSn bonding with relative dimensions is shown in Figure 7. If post-processing is needed, such as thinning after bonding, the percentage of the bonded surface area required to provide a strong bond can be significant. The eutectic micro-pillar bonding process may still represent too high a mass budget for high energy physics applications.

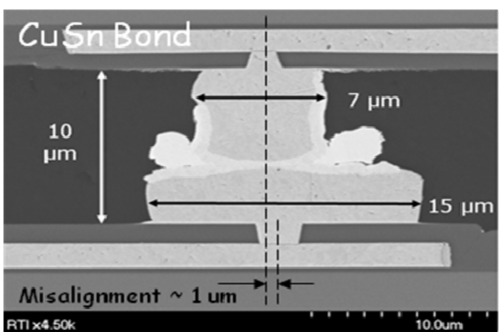

Fig. 7. Cross section of CuSn bond at fine pitch.

A second bonding technique that is being pursued is the Solid Liquid Inter-Diffusion (SLID) approach [22]. The contact pads on the sensor wafer are electroplated with copper and tin, the ROIC pads with copper. The wafers are aligned and flipped, the connection is made by heating to 300 ^{o}C when copper and tin form an alloy which melts at much higher temperatures (> 600 ^{o}C). A pitch of less than 20 μm can be achieved, limited by the precision of the wafer or chip alignment. Both wafer-to-wafer and chip-to-wafer bonding are possible. The SLID process is compatible with interchip vias and allows stacking of multiple layers. MPI Munich plans to connect existing hybrid pixel readout ROICs to high resistivity sensor wafers using this IZM SLID process [23]. The ROICs will be thinned and service connection will be provided from the backside using vias. Test connections made with sensor wafers and dummy ROICs showed high yield, the fraction of open connections was at the 10^{-4} level.

Another bonding technique that is being studied is the Direct Bond Interconnect (DBI) technology from Ziptronix [24], based on oxide bonding of wafers and chips with embedded metal to form the inter-layer contact. Minimal mass is required for bonding in this process. In the DBI process, patterned metal contact structures are deposited on the sensor and ROIC pixels. Silicon oxide is then deposited to cover the contact structures and wafer surface. Chemical-mechanical polish is used to planarize the wafer surface and expose the metal contacts. To form the initial oxide bond, wafers are carefully cleaned and their surfaces are activated by a chemical treatment. The sensor and readout are then aligned, with the metal contacts facing each other, and compressed. A final heating improves the inter-wafer bond strength and the metal-metal contact quality. Alignment accuracies of 1 μm have been achieved. The DBI technology has several advantages. Unlike bump-bonding where the interconnect pitch is limited by bump-to-bump shorts, the DBI technology allows very fine pitch. A pitch of 3 μm has been demonstrated. The DBI technology is also low mass. The DBI metal contacts have a height less than 1 μm and cover a very small fraction of the surface area. Furthermore, the bond is very strong. The technology allows for aggressive post-bond thinning, and can be used with wafers or individual die. Die can be placed with standard pick-and-place machines at room temperature, eliminating the multiple thermal cycles necessary for multi-chip solder bumping. The DBI technology can also be used in conjunction with the embedded through-silicon-vias available in the Tezzaron/Chartered technology to assembly a large area detector array that can be tiled with chips and contacted through the back side.

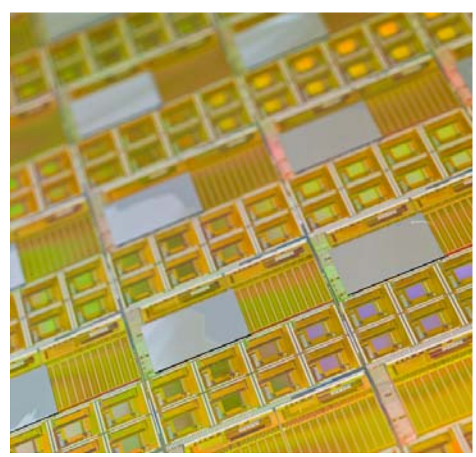

Fig. 8. Individual sensors bonded to a readout wafer using the DBI process after post-processing.

To demonstrate the DBI technology, 8" wafers with readout circuits for pixel detectors with a pitch of 50x400 μm^2 were bonded to individual 4-side buttable sensors with an array of 22×128 diodes on a high resistivity substrate. The sensors employ a 50 μm deep trench etch at the edge followed by doping of the sidewalls using poly-silicon to provide a high quality doped surface. This allows the anode, and thus the charge collection field, to be extended to the edge without excessive leakage current. After bonding, the sensors were thinned to 100 µm. Due to the large surface bonding area associated with the DBI process, there was no damage to the sensors during the thinning process. Thinning down to a sensor thickness of 50 µm should be possible. Figure 8 shows a photograph of individual pixel sensors DBI bonded to readout circuits on an 8" wafer using the DBI process after thinning. Initial test results show that all pixels were connected.

In the first run organized by the 3D-IC Consortium, multiple designs are included that provide only the front-end readout electronics and will have to be mated with sensors. The designs target very different science applications. Two designs are geared towards high energy physics applications. The first design is an adaptation of the Vertically Integrated Pixel (VIP) chip, referenced in Section II, adapted to the two-tier Tezzaron/Chartered process. Since there are only two tiers of electronics available, the pixel size of the 192x192 array has been increased to 24x24 µm^2. This design is aimed at the readout of a pixel detector for an electron-positron collider and features high speed data sparsification, high resolution digital time stamp and high speed token passing for readout [7]. A second design explores the feasibility of the 3D technology for the formation of a fast track trigger in a hadron collider environment. The track-trigger concept is based on a momentum filter utilizing a pair of silicon sensors separated by about 1 mm and interconnected vertically, allowing local processing of hit information. Figure 9 shows a sketch of the concept. A silicon sensor is DBI bonded to a readout chip, fabricated in a 3D process. First level processing is performed and the signals are transmitted, through an interposer, to a second pair of sensor and 3D readout circuit. The pattern of pixel hits in both sensors is compared and a decision is formed. Since the interconnect density of the readout circuit to the interposer is relatively small, conventional bump bonding could be considered for this connection. The initial goal is to demonstrate the assembly of a sensor-chip-interposer module with back-side contacts based on 3D and/or bump bonding and characterize the stack electrically.

Another design is aimed at evaluating the application of this technology for X-ray photon correlation spectroscopy to calculate the autocorrelation function per pixel. In the current design, the 3D readout chip operates in a dead-time-less fashion to record the arrival time of each photon in every pixel. The top tier of the two-tiered readout chip will be bonded to a sensor and handles the low-noise analog functions, and the bottom tier handles the digital event recording and time-stamping. The chip includes a 64 x 64 array of 80x80 µm^2 pixels with high speed sparsified data readout. The chip is adaptable to 4-side buttable X-ray detector arrays.

The sensors that will mate with these circuits are being fabricated in parallel. Production of sensors at X-FAB are being explored. Different bonding techniques will be exercised with these devices. Besides the ultra-fine pitch bump-bond and DBI technology, it is foreseen to test a metal bond with adhesive injection as proposed by ZyCube [20].

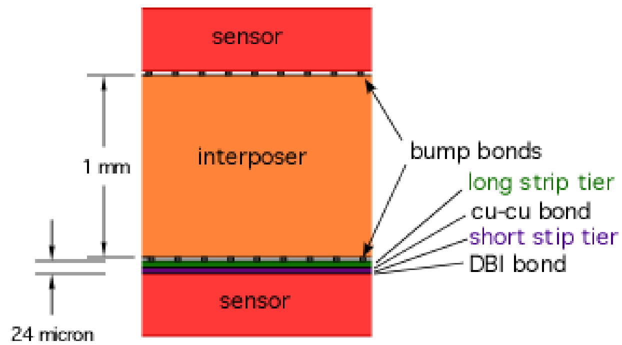

Fig. 9. Concept of a pair of sensor-readout circuit assemblies communicating with each other at high rate through an interposer.

V. The Facilitation Group for Monolithic and Vertically Integrated Pixel Detector R&D

3D integrated circuits will unquestionably play a critical role in the development of new detectors. The development of 3D integrated circuits, however, is a challenge for high energy physics applications and for science applications in general for a number of reasons. First of all, the cost can be prohibitively high, especially for smaller research institutions. Since the scientific community, especially in the R&D phase, is a very low volume customer, there is normally also limited access to foundries. Furthermore, there may be a mismatch between requirements from industry and high energy physics. To cope with the cost of engineering runs and to share efforts and experience in the design of vertically integrated devices, the community has organized itself in consortia among worldwide research institutions. The 3D-IC Consortium [8], promoted by Fermi National Accelerator Laboratory and which currently has 17 international partners, is one example of such an organization.

To provide additional service to existing and emerging collaborations and to enable quicker and more efficient development of pixel detector technologies for particle physics, this discipline has earlier this year established a facilitation group for monolithic and vertically integrated pixel detector R&D. Present members of this group are M. Demarteau (Fermilab, U.S.A.), J. Haba (KEK, Japan), H.-G. Moser (MPI, Germany), V. Re (INFN, Italy). By engaging other community members, this group is charged with the following tasks. In the first place, it is asked to investigate the expectations and needs of the monolithic and vertically integrated pixel community, to investigate the needs of other scientific communities interested in these technologies and to investigate the development of these technologies for applications other than particle physics. Its main goal is to foster collaboration across different pixel R&D groups to facilitate the development of these new and promising technologies for high energy physics applications by provide a means of networking and exchange of information between groups. It is thought that through the development of an effective network between R&D collaborations working in this field, by establishing and coordinating contacts to foundries, research institutes and industry, the group will provide an additional service to the community that will facilitate and expedite the development of these new technologies. The facilitation group will not direct the effort and direction of individual R&D projects.

The facilitation group is currently exploring how to best serve the community and interact with existing consortia. Areas that are being explored are opportunities for funding, shared and common infrastructure for testing, offering successful implementations of new technologies to the community at large and, of course, facilitate ways in which members can meet and exchange information.

New technologies have always presented challenges to the field of science. At the same time, experience shows that successes with new technologies have often led to dramatic advances in science reach. Today, industry is making rapid progress in developing vertically integrated circuits. The field of high energy physics has responded with new initiatives and the formation of consortia to explore this technology. The formation of a facilitation group for monolithic and vertically integrated pixel detector R&D provides an additional service to the community with the ultimate goal of enabling this technology on a faster pace to a larger segment of the community for the next generation of science experiments.

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